
Reverse-Engineered Datasheet PowerVR SGX544 Documentation

Release 1.0

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Nov 03, 2018

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CHAPTER 1

Introduction

CHAPTER 2

Features of PVR SGX544MP

Infos from sgxfeaturedefs.h

- Autoclockgating

CHAPTER 3

Reverse Engineering Tools

CHAPTER 4

Acronyms and abbreviations

Abbreviation	Long Name	Explanantion
USSE or USE	Universal Scalable Shader Engine	
BIF	Bus Interface	
VDM	Vertex data master	
PDS	Programmable data sequencer	
ISP	Image Synthesis Processor	
TSP	Texture and Shader setup Processor	
TE	Tiling Engine	
MTE	Macro Tiling Engine	
DPM	Dynamic Parameter Management	
TA	Tiling Accelerator	
PBE	Pixel Back End	
TCU	Texture Cache Unit	
DCU	Data Cache Unit	
ITR	Iterator	

CHAPTER 5

Register List

These information come from Published code from Img Tech and is under the GPL v2 Licence. According to the Datasheet of the A83T the Registers have a total size of 64k (Adressrange: 0x0000 - 0xFFFF)

Register Name	Offset	Description
CLKGATECTL	0x0000	Clock Gate Control Register
CLKGATECTL2	0x0004	Clock Gate Control Register2
CLKGATESTATUS	0x0008	Clock Gate Status Register
CLKGATECTLOVR	0x000C	Clock Gate -?- Register
POWER	0x001C	Power Register
CORE_ID	0x0020	Core ID Register
CORE_REVISION	0x0024	Core Revision Register
DESIGNER_REV_FIELD1	0x0028	Designer Revision Field 1 Register
DESIGNER_REV_FIELD2	0x002C	Designer Revision Field 2 Register
SOFT_RESET	0x0080	Soft Reset Register
EVENT_HOST_ENABLE2	0x0110	Event Host Enable Register 2
EVENT_HOST_CLEAR2	0x0114	Event Host Clear Register 2
EVENT_STATUS2	0x0118	Event Status Register 2
EVENT_STATUS1	0x012C	Event Status Register 1
EVENT_HOST_ENABLE1	0x0130	Event Host Enable Register 1
HOST_CLEAR1	0x0134	Event Host Clear Register 1
TIMER	0x0144	Timer Register
EVENT_KICK1	0x0AB0	Event Kick 1 Register
EVENT_KICK2	0x0AC0	Event Kick 2 Register
EVENT_KICKER	0x0AC4	Event Kicker Register
EVENT_KICK0	0x0AC8	Event Kick 0 Register
EVENT_TIMER	0x0ACC	Event Timer Register

Continued on next page

Table 1 – continued from previous page

Register Name	Offset	Description
PDS_INV0	0x0AD0	-?-
PDS_INV1	0x0AD4	-?-
EVENT_KICK3	0x0AD8	Event Kick 3 Register
PDS_INV3	0x0ADC	-?-
PDS_INV_CSC	0x0AE0	-?-
BIF_CTRL	0x0C00	BIF Control Register
BIF_INT_STAT	0x0C04	BIF INT Status Register
BIF_FAULT	0x0C08	BIF Fault Register
BIF_TILE0	0x0C0C	BIF Tile 0 Register
BIF_TILE1	0x0C10	BIF Tile 1 Register
BIF_TILE2	0x0C14	BIF Tile 2 Register
BIF_TILE3	0x0C18	BIF Tile 3 Register
BIF_TILE4	0x0C1C	BIF Tile 4 Register
BIF_TILE5	0x0C20	BIF Tile 5 Register
BIF_TILE6	0x0C24	BIF Tile 6 Register
BIF_TILE7	0x0C28	BIF Tile 7 Register
BIF_TILE8	0x0C2C	BIF Tile 8 Register
BIF_TILE9	0x0C30	BIF Tile 9 Register
BIF_CTRL_INVALID	0x0C34	BIF Control INVALID Register
BIF_DIR_LIST_BASE1	0x0C38	-?-
BIF_DIR_LIST_BASE2	0x0C3C	-?-
BIF_DIR_LIST_BASE3	0x0C40	-?-
BIF_DIR_LIST_BASE4	0x0C44	-?-
BIF_DIR_LIST_BASE5	0x0C48	-?-
BIF_DIR_LIST_BASE6	0x0C4C	-?-
BIF_DIR_LIST_BASE7	0x0C50	-?-
BIF_BANK_SET	0x0C74	BIF Bank Set Register
BIF_BANK0	0x0C78	BIF Bank 0 Register
BIF_BANK1	0x0C7C	BIF Bank 1 Register
BIF_DIR_LIST_BASE0	0x0C84	-?-
BIF_TA_REQ_BASE	0x0C90	-?-
BIF_MEM_REQ_STAT	0x0CA8	-?-
BIF_3D_REQ_BASE	0x0CAC	-?-
BIF_ZLS_REQ_BASE	0x0CB0	-?-
BIF_BANK_STATUS	0x0CB4	-?-
BIF_MMU_CTRL	0x0CD0	-?-
2D_BLIT_STATUS	0x0E04	2D BLIT Status Register
2D_VIRTUAL_FIFO_0	0x0E10	-?-
2D_VIRTUAL_FIFO_1	0x0E14	-?-
BREAKPOINT0_START	0x0F44	-?-
BREAKPOINT0_END	0x0F48	-?-
BREAKPOINT0	0x0F4C	-?-
BREAKPOINT1_START	0x0F50	-?-
BREAKPOINT1_END	0x0F54	-?-

Continued on next page

Table 1 – continued from previous page

Register Name	Offset	Description
BREAKPOINT1	0x0F58	-?-
BREAKPOINT2_START	0x0F5C	-?-
BREAKPOINT2_END	0x0F60	-?-
BREAKPOINT2	0x0F64	-?-
BREAKPOINT3_START	0x0F68	-?-
BREAKPOINT3_END	0x0F6C	-?-
BREAKPOINT3	0x0F70	-?-
BREAKPOINT_READ	0x0F74	-?-
PARTITION_BREAKPOINT_TRAP	0x0F78	-?-
PARTITION_BREAKPOINT	0x0F7C	-?-
PARTITION_BREAKPOINT_TRAP_INFO0	0x0F80	-?-
PARTITION_BREAKPOINT_TRAP_INFO1	0x0F84	-?-
USE_CODE_BASE_0	0x0A0C	USE Code Base Register 0
USE_CODE_BASE_1	0x0A10	USE Code Base Register 1
USE_CODE_BASE_2	0x0A14	USE Code Base Register 2
USE_CODE_BASE_3	0x0A18	USE Code Base Register 3
USE_CODE_BASE_4	0x0A1C	USE Code Base Register 4
USE_CODE_BASE_5	0x0A20	USE Code Base Register 5
USE_CODE_BASE_6	0x0A24	USE Code Base Register 6
USE_CODE_BASE_7	0x0A28	USE Code Base Register 7
USE_CODE_BASE_8	0x0A2C	USE Code Base Register 8
USE_CODE_BASE_9	0x0A30	USE Code Base Register 9
USE_CODE_BASE_10	0x0A34	USE Code Base Register 10
USE_CODE_BASE_11	0x0A38	USE Code Base Register 11
USE_CODE_BASE_12	0x0A3C	USE Code Base Register 12
USE_CODE_BASE_13	0x0A40	USE Code Base Register 13
USE_CODE_BASE_14	0x0A44	USE Code Base Register 14
USE_CODE_BASE_15	0x0A48	USE Code Base Register 15
PIPE0_BREAKPOINT_TRAP	0x0F88	Pipe 0 Breakpoint Trap Register
PIPE0_BREAKPOINT	0x0F8C	Pipe 0 Breakpoint Register
PIPE0_BREAKPOINT_TRAP_INFO0	0x0F90	Pipe 0 Breakpoint Trap Info Register 0
PIPE0_BREAKPOINT_TRAP_INFO1	0x0F94	Pipe 0 Breakpoint Trap Info Register 1
PIPE1_BREAKPOINT_TRAP	0x0F98	Pipe 1 Breakpoint Trap Register
PIPE1_BREAKPOINT	0x0F9C	Pipe 1 Breakpoint Register
PIPE1_BREAKPOINT_TRAP_INFO0	0x0FA0	Pipe 1 Breakpoint Trap Info Register 0
PIPE1_BREAKPOINT_TRAP_INFO1	0x0FA4	Pipe 1 Breakpoint Trap Info Register 1

Register List SGX544

Register Name	Offset	Description
MASTER_BIF_CTRL	0x4C00	Master BIF Control Register
MASTER_BIF_INIT_STAT	0x4C04	Master BIF -?- Register

Register List MP Master

CHAPTER 6

Registers

Offset:			Registername: REGISTER_NAME
Bit:	R/W:	Default/Hex	Description:
31:0	R/W	0xFFFFFFFF	
31:0	R/W	0x0	

6.1 Clock Gate Control Register [CLKGATECTL] (Default Value: 0xFFFFFFFF)

Offset: 0x0000			Registername: CLKGATECTL
Bit:	R/W:	Default/Hex	Description
31:29	/	0x0	/
28	R/W	0x0	CLKGATECTL_SYSTEM_CLKG • 0: • 1:
27:25	/	0x0	/
24	R/W	0x0	CLKGATECTL_AUTO_MAN_RE • 0: • 1:
23:22	/	0x0	/
21:20	R/W	0x0	CLKGATECTL_BIF_CORE_CLK • 0x0: • 0x1: • 0x2:
19:18	R/W	0x0	CLKGATECTL_TA_CLKG • 0x0: • 0x1: • 0x2:
17:16	R/W	0x0	CLKGATECTL_IDXFIFO_CLKG • 0x0: • 0x1: • 0x2:
15:14	R/W	0x0	CLKGATECTL_PDS_CLKG • 0x0: • 0x1: • 0x2:
13:12	R/W	0x0	CLKGATECTL_VDM_CLKG • 0x0: • 0x1:

6.1. Clock Gate Control Register [CLKGATECTL] (Default Value: 0xFFFFFFFF)

6.2 Clock Gate Control Register 2 [CLKGATECTL2](Default Value: 0xFFFFFFFF)

Offset: 0x0004			Registername: CLKGATECTL2
Bit:	R/W:	Default/Hex	Description
31:28	R/W	0x0	/
27:26	R/W	0x0	CLKGATECTL2_DCU0_L0L1_CLKG • 0x0: • 0x1: • 0x2:
25:24	R/W	0x0	CLKGATECTL2_DCU1_L0L1_CLKG • 0x0: • 0x1: • 0x2:
23:22	R/W	0x0	CLKGATECTL2_DCU_L2_CLKG • 0x0: • 0x1: • 0x2:
21:20	R/W	0x0	/
19:18	R/W	0x0	CLKGATECTL2_TEX1_CLKG • 0x0: • 0x1: • 0x2:
17:16	R/W	0x0	CLKGATECTL2_ITR1_CLKG • 0x0: • 0x1: • 0x2:
15:14	R/W	0x0	CLKGATECTL2_USE1_CLKG • 0x0: • 0x1: • 0x2:
13:12	R/W	0x0	CLKGATECTL2_TEX0_CLKG • 0x0: • 0x1: • 0x2:
6.2.1 Clock Gate Control Register 2 [CLKGATECTL2](Default Value: 0xFFFFFFFF)			Value: 19
	R/W	0x0	CLKGATECTL2_TEX0_CLKG

6.3 Clock Gate Status Register [CLKGATESTATUS](Default Value: 0xFFFFFFFF)

Offset: 0x0008			Registername: CLKGATESTATUS
Bit:	R/W:	Default/Hex	Description
31:25	R/W	0x0	/
24	R/W	0x0	CLKGATESTATUS_BIF_CORE_CLKS
23	R/W	0x0	CLKGATESTATUS_DCU1_L0L1_CLKS
22	R/W	0x0	CLKGATESTATUS_DCU0_L0L1_CLKS
21	R/W	0x0	CLKGATESTATUS_DCU_L2_CLKS
20	R/W	0x0	CLKGATESTATUS_TA_CLKS
19	R/W	0x0	CLKGATESTATUS_IDXFIFO_CLKS
18	R/W	0x0	/
17	R/W	0x0	CLKGATESTATUS_TEX1_CLKS
16	R/W	0x0	CLKGATESTATUS_ITR1_CLKS
15	R/W	0x0	CLKGATESTATUS_USE1_CLKS
14	R/W	0x0	/
13	R/W	0x0	CLKGATESTATUS_TEX0_CLKS
12	R/W	0x0	CLKGATESTATUS_ITR0_CLKS
11	R/W	0x0	CLKGATESTATUS_USE0_CLKS
10	R/W	0x0	CLKGATESTATUS_UCACHEL2_CLKS
9	R/W	0x0	CLKGATESTATUS_TCU_L2_CLKS
8	R/W	0x0	CLKGATESTATUS_PBE_CLKS
7	R/W	0x0	CLKGATESTATUS_PDS_CLKS
6	R/W	0x0	CLKGATESTATUS_VDM_CLKS
5	R/W	0x0	CLKGATESTATUS_DPM_CLKS
4	R/W	0x0	CLKGATESTATUS_MTE_CLKS
3	R/W	0x0	CLKGATESTATUS_TE_CLKS
2	R/W	0x0	CLKGATESTATUS_TSP_CLKS
1	R/W	0x0	CLKGATESTATUS_ISP2_CLKS
0	R/W	0x0	CLKGATESTATUS_ISP_CLKS

6.4 Clock Gate -?- Register [CLKGATECTLOVR](Default Value: 0xFFFFFFFF)

Offset: 0x000C			Registername: CLKGATECTLOVR
Bit:	R/W:	Default/Hex	Description
31:22	R/W	0x0	/
21:20	R/W	0x0	CLKGATECTLOVR_BIF_CORE_CLKO
19:18	R/W	0x0	CLKGATECTLOVR_TA_CLKO
17:16	R/W	0x0	CLKGATECTLOVR_IDXFIFO_CLKO
15:14	R/W	0x0	CLKGATECTLOVR_PDS_CLKO
13:12	R/W	0x0	CLKGATECTLOVR_VDM_CLKO
11:10	R/W	0x0	CLKGATECTLOVR_DPM_CLKO
9:8	R/W	0x0	CLKGATECTLOVR_MTE_CLKO
7:6	R/W	0x0	CLKGATECTLOVR_TE_CLKO
5:4	R/W	0x0	CLKGATECTLOVR_TSP_CLKO
3:2	R/W	0x0	CLKGATECTLOVR_ISP2_CLKO
1:0	R/W	0x0	CLKGATECTLOVR_ISP_CLKO

6.5 Power Register [POWER](Default Value: 0x00000000)

Offset: 0x001C			Registername: POWER
Bit:	R/W:	Default/Hex	Description
31:0	/	0x00000000	/
0	R/W	0x0	POWER_PIPE_DISABLE Disables ? * 0: Disable ? * 1: Enable ?

6.6 Core ID Register [CORE_ID](Default Value: 0xFFFFFFFF)

Offset: 0x0020			Registername: CORE_ID
Bit:	R/W:	Default/Hex	Description:
31:16	R	/	CORE_ID_ID
15:12	R	/	CORE_ID_CONFIG_SLC
11:8	R	/	CORE_ID_CONFIG_CORES
7:2	R	/	CORE_ID_CONFIG
1	R	/	CORE_ID_CONFIG_BASE
0	R	/	CORE_ID_CONFIG_MULTI

6.7 Core Revision Register [CORE_REVISION](Default Value: 0XXXXXXXXX)

Offset: 0x0024			Registername: CORE_REVISION
Bit:	R/W:	Default/Hex	Description:
31:24	R	/	CORE_REVISION_DESIGNER
23:16	R	/	CORE_REVISION_MAJOR
15:8	R	/	CORE_REVISION_MINOR
7:0	R	/	CORE_REVISION_MAINTENANCE

Revision : Major.Minor.Maintenance

Manufacturer	Device	Revision
Allwinner	A83T	1.1.5
Allwinner	A31	
Actions	S500	

6.8 Core Revision Field 1 Register [CORE_REV_FIELD1](Default Value: 0XXXXXXXXX)

Offset: 0x0028			Registername: CORE_REV_FIELD1
Bit:	R/W:	Default/Hex	Description
31:0	/	/	DESIGNER_REV_FIELD1_DESIGNER_REV_FIELD1

6.9 Core Revision Field 2 Register [DESIGNER_REV_FIELD2](Default Value: 0XXXXXXXXX)

Offset: 0x002C			Registername: DESIGNER_REV_FIELD2
Bit:	R/W:	Default/Hex	Description
31:0	R	/	DESIGNER_REV_FIELD2_DESIGNER_REV_FIELD2

6.10 Soft Reset Register [SOFT_RESET](Default Value: 0x00000000)

Offset: 0x0080			Registername: SOFT_RESET
Bit:	R/W:	Default/Hex	Description:
31:20	R/W	0x000	/
19	R/W	0x0	SOFT_RESET_DCU_L0L1_RESET
18	R/W	0x0	SOFT_RESET_DCU_L2_RESET
17	R/W	0x0	SOFT_RESET_TA_RESET
16	R/W	0x0	SOFT_RESET_IDXFIFO_RESET
15	R/W	0x0	SOFT_RESET_USE_RESET
14	R/W	0x0	SOFT_RESET_TEX_RESET
13	R/W	0x0	SOFT_RESET_ITR_RESET
12	R/W	0x0	/
11	R/W	0x0	SOFT_RESET_UCACHEL2_RESET
10	R/W	0x0	SOFT_RESET_TCU_L2_RESET
9	R/W	0x0	SOFT_RESET_PBE_RESET
8	R/W	0x0	SOFT_RESET_PDS_RESET
7	R/W	0x0	SOFT_RESET_TSP_RESET
6	R/W	0x0	SOFT_RESET_ISP2_RESET
5	R/W	0x0	SOFT_RESET_ISP_RESET
4	R/W	0x0	SOFT_RESET_MTE_RESET
3	R/W	0x0	SOFT_RESET_TE_RESET
2	R/W	0x0	SOFT_RESET_DPM_RESET
1	R/W	0x0	SOFT_RESET_VDM_RESET
0	R/W	0x0	SOFT_RESET_BIF_RESET

CHAPTER 7

Indices and tables

- `genindex`
- `modindex`
- `search`