

The diagram illustrates the timing of the OUT signal relative to the input signals INPA, INPB, INPC, INPD, and INPE. The OUT signal is high during the first two clock ticks (0-1) and the eleventh clock tick (11), and low during the remaining clock ticks (2-10 and 12-14). The input signals INPA, INPB, INPC, INPD, and INPE are active-low, with INPA, INPB, INPC, INPD, and INPE being high from tick 5 to 10. The OUT signal is low from tick 0 to 1 and from tick 6 to 10, and high from tick 11 to 12.

OUT

Timestamp (125MHz FPGA clock ticks)